

Near-Ideal Si-SiO₂ Interfaces

The Si-SiO₂ interface plays a key role in insulated-gate field-effect transistors (IGFETs). Of principal concern are the interface charge density Q_{ic} and the fast-state density N_{fs} . These properties can be optimized by eliminating the transition region and creating an abrupt interface. Our work with the chemical vapor deposition (CVD) of SiO₂ using a CO₂-SiH₄-H₂ system in the presence or absence of trace amounts of HCl gas at 1000°C has demonstrated that unannealed CVD SiO₂ on (100) Si using a vertical-cold-wall reactor has properties similar to those of unannealed SiO₂ on (100) Si formed by the usual thermal oxidation procedure. In addition, using only 2.27 vol% HCl, we have produced films of SiO₂ on (111) Si that are better than their thermal counterparts, unannealed or annealed; i.e., $Q_{ic} \approx 5 \times 10^{10} \text{ cm}^{-2}$ and $N_{fs} \approx 10^{10} \text{ cm}^{-2} \cdot \text{eV}^{-1}$. We attribute these results, at least in part, to an abrupt interface between the CVD SiO₂ and Si. Deposition rates of 10–20 nm/min were used to reproducibly deposit 30–50 nm of SiO₂. The CVD SiO₂ films also show a significantly lower standard deviation in the breakdown fields ($\pm 1.5\%$) and the mobile charge densities ($\pm 5\%$) than their thermal counterparts. In general, N_{fs} was independent of Q_{ic} .

Introduction

Silicon dioxide (SiO₂) is the standard insulator used for metal and silicon gate insulated-gate field-effect transistors (IGFETs) and as such, has undergone intensive material studies. For these device applications, one is typically concerned with the fixed charge density Q_{ss} in the bulk of the material and the fast-surface-state density N_{fs} at the Si-SiO₂ interface. These properties help to define the threshold voltage and current, respectively, in the active portion of the device (i.e., the channel).

The SiO₂ is usually formed by thermal oxidation of Si, a well-known diffusion-limited process whereby oxygen migrates through the SiO₂ to the Si-SiO₂ interface and reacts with Si to form additional SiO₂ [1]. This process is known to cause point defects in the Si as well as residual excess Si in the SiO₂ at the interface. This non-stoichiometric condition at both the interface and within the bulk SiO₂ manifests itself as missing Si atoms (vacancies) on the Si side of the interface, as dangling Si and O bonds on the SiO₂ side of the interface, and as Si-Si bonds (excess Si) in the SiO₂.

The excess Si in the bulk oxide and at the interface determines the fixed charge density Q_{ss} [2], while the missing, dangling, and extra bonds at or near the interface de-

termine the fast-surface-state density N_{fs} [3]. Laughlin *et al.* [3] also demonstrated that theoretically one can create a perfectly abrupt Si-SiO₂ interface with no fast states. This is typically done by means of a post-oxidation anneal (not surprising when one considers that post-oxidation annealing is usually used to reduce both Q_{ss} and N_{fs}). In fact, our CVD process eliminates the need for a post-deposition anneal, which would certainly simplify subsequent processing.

The objective of this paper is to demonstrate that chemical vapor deposition (CVD) of SiO₂ on Si at 1000°C can result in a near-ideal oxide and interface without the use of a high-temperature annealing step on both (100) and (111) Si substrates. By comparing values for properties such as Q_{ss} , N_{fs} , the interface charge density Q_{ic} , etc., for both unannealed thermal and CVD SiO₂ films, we show that this process may be useful in the fabrication of IGFETs as well as bipolar devices because of the control of the Si-SiO₂ interface on both (100) and (111) Si.

Deposition conditions and physical properties of CVD SiO₂

In order to bring about structural ideality, there must be sufficient thermal energy available and the resultant SiO₂

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must be stoichiometric. In addition, the oxidant used should not react at high temperatures with the Si substrate used in the CVD deposition. These requirements were met through the use of silane (SiH_4) as the reactant, CO_2 as the oxidant, and H_2 as the carrier gas. The SiO_2 was deposited on Si wafers placed on the surface of an induction-heated carbon susceptor placed inside a vertical-cold-wall barrel reactor [4]. Early experiments with this system gave nonideal films with high fixed-charge densities Q_{ss} . It was determined that this was a result of decomposition of the SiH_4 to give free Si (and H_2), which was then incorporated into the SiO_2 films. Therefore, trace amounts of gaseous HCl were introduced during the deposition process in order to convert this free Si into a volatile material (SiH_3Cl_y) [5]. As a result, the fixed-charge densities of the films were essentially eliminated and a concurrent reduction in the deposition rate from 20 to 13 nm/min was observed. The typical H_2 flow rate was $0.1 \text{ m}^3/\text{min}$, the mole fractions of SiH_4 and CO_2 were 2×10^{-4} and 1×10^{-2} , respectively, and the HCl was used in 0.27 vol%. The deposited film thicknesses in the presence and absence of HCl were 33–200 nm and 50–300 nm (both $\pm 5\%$), respectively.

In order to make comparisons with thermal SiO_2 , both n- and p-type Si substrates were used in both (100) and (111) surface orientations. Typical values of Q_{ss} and N_{fs} that we obtained for thermally oxidized SiO_2 after an optimized high-temperature anneal were: (100) Si – $2 \times 10^{10} \text{ cm}^{-2}$, $3 \times 10^{10} \text{ cm}^{-2}\text{-eV}^{-1}$; (111) Si – $1 \times 10^{11} \text{ cm}^{-2}$, $1 \times 10^{11} \text{ cm}^{-2}\text{-eV}^{-1}$, respectively. [In fact, the dependence of these properties on the surface orientation has generally led to the choice of (100) Si for IGFET device fabrication, while (111) Si is generally used for bipolar devices; however, IBM uses (100) Si for both of these.] For unannealed films, Q_{ss} for (111) Si is generally not lower than $1.5\text{--}2.0 \times 10^{11} \text{ cm}^{-2}$ and N_{fs} is quite often $< 1 \times 10^{10} \text{ cm}^{-2}\text{-eV}^{-1}$ for (100) Si; N_{fs} is typically $< 1 \times 10^{11} \text{ cm}^{-2}\text{-eV}^{-1}$ for (111) Si after a proper low-temperature anneal [6]. A comparison of the physical properties obtained for high-temperature-annealed thermal and unannealed CVD SiO_2 on (100) Si are shown in Table 1. The indices of refraction, etch rates, densities, breakdown fields, and dielectric constants are all similar. Although the breakdown fields are similar for both types of oxide, we observed [7] a significantly lower standard deviation in the breakdown fields for CVD SiO_2 ($\pm 1.5\%$) compared with the thermal SiO_2 ($\pm 20\%$). The fixed, mobile, and fast-surface-state charge densities are lower in the CVD oxide and more readily controlled.

In particular, the mobile charge densities typically achieved with this CVD system are very low (see Table 1) and can be routinely controlled. This relatively easy con-

Table 1 A comparison of the properties obtained for high-temperature-annealed thermal SiO_2 and unannealed CVD SiO_2 on (100) Si; thermal oxidation at 1000°C in dry O_2 ; CVD oxide deposited at 1000°C .

Property	Thermal	CVD
Refractive index (546 nm)	1.462	1.45–1.46
Etch rate on p-etch (nm/s)	20.6	28–30
Density (g/cm^3)	≈ 2.27	2.2–2.3
Fixed charge density, Q_{ss} (cm^{-2})	$2\text{--}5 \times 10^{10}$	$< 1 \times 10^{10}$
Mobile charge density (cm^{-2})	$0.2\text{--}1 \times 10^{10}$	$\approx 2 \times 10^{10}$
Fast-surface-state density, N_{fs} ($\text{cm}^{-2}\text{-eV}^{-1}$)	$2\text{--}10 \times 10^{10}$ ($< 1 \times 10^{10}$) [*]	1.5×10^{10}
Breakdown field† ($\text{V}\cdot\text{cm}^{-1}$)	$7\text{--}9 \times 10^6$	$7\text{--}9 \times 10^6$
Standard deviation in breakdown field (%)	± 20	± 1.5
Dielectric constant	3.9	3.8–4.0

^{*}Value for low-temperature-annealed material [6].
[†]100-nm films.

trol of the mobile charge density, compared to the case with most thermally oxidized SiO_2 films, is possibly due to the nature of the vertical-cold-wall reactor we used. Only the susceptor upon which the wafer rests is heated, while the walls of the system are kept at $\approx 300^\circ\text{C}$. On the other hand, it is well known that high mobile charge densities result from thermal oxidation processes, which take place in a quartz tube *inside* a furnace. Since the furnace and tube are at high temperatures, any impurities in the furnace, oxidation tube, or wafers can contaminate the process.

Fixed charge in high-temperature CVD SiO_2

An accurate measure of the true fixed charge at the interface Q_{ic} , as measured in MOS (metal-oxide-silicon) structures, requires determination of the normalized metal-to-silicon work function Φ_{ms} . This term is a function of the doping level (cm^{-3}) of donors N_d or acceptors N_a for n- or p-type silicon, respectively, the absolute temperature T (K), and the electron affinity of Si, χ_{Si} . We have previously determined these constants for the CVD SiO_2 system [7]; Φ_{ms} can be calculated from the difference between the work function of the metal ϕ_m and χ_{Si} .

The MOS equations relating Q_{ic} and the flatband voltage V_{fb} (as measured from C-V curves) are as follows:

$$V_{fb} + \phi_n = \frac{\Phi_{ms}}{q} - \frac{Q_{ic}d_{ox}}{\epsilon_{ox}} - \frac{\rho_{ox}d_{ox}^2}{2\epsilon_{ox}} \quad (\text{n-type Si}), \quad (1)$$

$$V_{fb} - \phi_p = \frac{\Phi_{ms} - E_g}{q} - \frac{Q_{ic}d_{ox}}{\epsilon_{ox}} - \frac{\rho_{ox}d_{ox}^2}{2\epsilon_{ox}} \quad (\text{p-type Si}), \quad (2)$$

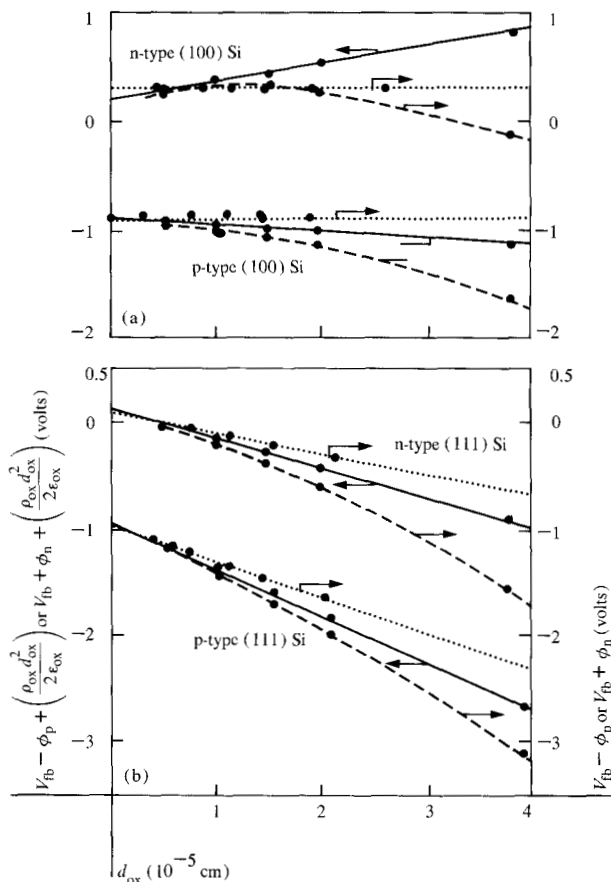


Figure 1 Plots of Eqs. (1) and (2) including (dashed lines) and excluding (solid lines) bulk charge density terms versus oxide thickness for CVD SiO₂ deposited in the absence and presence (dotted lines) of HCl for (a) (100) Si and (b) (111) Si substrates.

where

$$\phi_n = (kT/q) \ln (N_c/N_d), \quad (3)$$

$$\phi_p = (kT/q) \ln (N_v/N_a), \quad (4)$$

E_g is the bandgap energy, ρ_{ox} is the bulk charge density in SiO₂ (cm⁻³), d_{ox} is the SiO₂ thickness (cm), ϵ_{ox} is the permittivity of the oxide, k is Boltzmann's constant, N_c and N_v are the density of states (cm⁻³) in the conduction and valence bands. The validity of Eqs. (1) and (2) is demonstrated in Fig. 1, where raw data are plotted for CVD SiO₂ deposited without HCl for substrates of n- and p-type (100) Si [Fig. 1(a)] and n- and p-type (111) Si [Fig. 1(b)]. The dashed lines are plots of $V_{fb} + \phi_n$ (or $V_{fb} - \phi_p$) versus d_{ox} ; the curvature indicates the presence of a uniform bulk charge density ρ_{ox} . Replotting the data with the bulk charge removed (solid lines) allows one to measure Q_{ic} from the slope of the line, and Φ_{ms} from the intercept.

Table 2 Values of ρ_{ox} (10¹⁵ cm⁻³), Q_{ic} (10¹⁰ cm⁻²), and Φ_{ms} (or $\Phi_{ms} - E_g$) (eV) for CVD SiO₂ deposited in the presence and absence of 0.27 vol% HCl gas.

Si type and orientation	Φ_{ms} or $\Phi_{ms} - E_g$		Q_{ic}		ρ_{ox}
	no HCl	HCl	no HCl	HCl	no HCl
n (100)	0.194 ±0.02	0.276 ±0.02	-3.4	≈0	2.74
n (111)	0.103 ±0.01	0.101 ±0.01	5.8	4.6	1.88
p (100)	-0.915 ±0.03	-0.926 ±0.01	1.1	≈0	1.50
p (111)	-0.955 ±0.02	-0.965 ±0.01	9.4	7.5	1.24
				mean	1.84

Table 2 summarizes the values obtained for Φ_{ms} , ρ_{ox} , and Q_{ic} for the CVD SiO₂ system without HCl.

Introduction of trace amounts of HCl gas to the CVD SiO₂ system eliminates ρ_{ox} , as evidenced by the absence of curvature in the dotted lines in Figs. 1(a) and (b). The zero slope for the data on (100) Si indicates $Q_{ic} = 0$. The values for Φ_{ms} and Q_{ic} for the CVD SiO₂ system with HCl are also summarized in Table 2.

The observed systematic dependence of Φ_{ms} on the surface orientation of the Si has been noted previously [7] and was found to depend on chemisorption of hydrogen at the Si-SiO₂ interface.

The flatband voltage, and as such the threshold voltage of an IGFET at the onset of inversion, is traditionally controlled by means of doping level, oxide thickness, and/or choice of electrode material. We have now demonstrated a deposition technique that can be used to reproducibly control V_{fb} via both Q_{ic} and ρ_{ox} , thus providing designers with additional degrees of freedom in IGFET design.

Fast surface states in high-temperature CVD SiO₂

The presence of fast surface states leads to reduced channel currents in IGFETs and therefore must be minimized for optimum device performance. The Si-SiO₂ interface created with CVD SiO₂ is believed to be extremely abrupt since typical deposition times for 50–100 nm of SiO₂ at 1000°C in the absence of oxygen are 3–6 min. For such rapid deposition, little diffusion is expected. This abrupt interface results in very low fast-state surface densities N_{fs} .

The standard model used for fast states requires the existence of two types of fast states [8]: one type that is

neutral above the Fermi level E_F and negative (by virtue of an accepted electron) below it (see Fig. 2); the other is positive above E_F and neutral (by virtue of an accepted electron) below it. Notice that both types of fast states accept electrons and that the relative population of each type depends on the position of E_F .

By cooling to 77 K, one can measure a flatband shift ΔV_{fb} that contains all the charge due to one type of fast state (e.g., all negative N_{fs} on n-type Si). This is different from the Gray-Brown technique [9], which does not account for changes in the Fermi level or the flatband capacitance C_{fb} . The integrated fast-state density N'_{fs} then becomes

$$N'_{fs} = \Delta V_{fb} \left| \frac{296 \text{ K}}{77 \text{ K}} - \Delta E_F \right| \frac{296 \text{ K}}{77 \text{ K}}, \quad (5)$$

where ΔE_F is the change in the Fermi level.

Care must be taken to correct for the true flatband capacitance at which the flatband voltage is measured since C_{fb} is also a function of temperature:

$$C_{fb} = (\epsilon_{ox} C_{ox}) / \left[d_{ox} + \frac{\epsilon_{ox}}{\epsilon_{Si}} \left(\frac{kT \epsilon_{Si} \epsilon_0}{Nq^2} \right)^{1/2} \right], \quad (6)$$

where $C_{ox} = \epsilon_0 \epsilon_{ox} / d_{ox} = \epsilon_{ox} / d_{ox}$, ϵ_0 being the permittivity of free space, ϵ_{ox} and ϵ_{Si} the dielectric constants of SiO_2 and Si, and N the doping level (N_a or N_d).

Typical 1-MHz (high-frequency) C - V curves at room temperature and 77 K, from which N'_{fs} can be measured, are shown in Fig. 3(a). We observed no distortions in these curves and very low fast-state densities. As a routine cross-check, low- and high-frequency C - V curves were compared to determine the midgap fast-state density at room temperature (296 K). A typical low-frequency curve is shown as a solid line in Fig. 3(b). Again, extremely low fast-state densities ($\approx 1 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$) were observed, as evidenced by the virtual superposition of the low- and high-frequency C - V curves in depletion.

The actual fast-state density near midgap can be calculated from

$$N_{fs} = \frac{C_{fs}}{q} = \frac{1}{q} \left[\frac{C_{lf} C_{ox}}{C_{ox} - C_{lf}} - \frac{C_{hf} C_{ox}}{C_{ox} - C_{hf}} \right], \quad (7)$$

where N_{fs} is the fast-surface-state density ($\text{cm}^{-2} \text{ eV}^{-1}$) near midgap, C_{fs} is the fast-state capacitance, and C_{lf} and C_{hf} are the low- and high-frequency capacitances. Usually N_{fs} is reported in graphic or tabular form from flatband to the onset of inversion. In this paper, we present the average value of N_{fs} at midgap, $\bar{N}_{fs}$. By summing N'_{fs} for n- and p-type Si, we have a measure of the total fast-state density ΣN_{fs} .

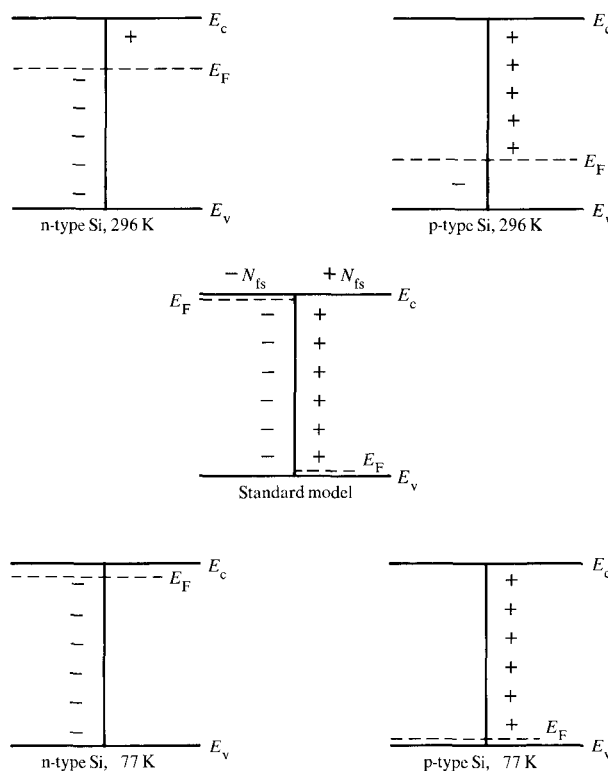


Figure 2 Standard model for fast surface states, indicating the relative populations at room temperature (296 K) and at 77 K. The symbols E_c , E_F , and E_v represent the energy levels of the conduction band, the Fermi level, and the valence band, respectively.

Measurements of N_{fs} and N'_{fs} were made on n- and p-type Si of both (100) and (111) orientations [10]. Samples were deposited in the presence and absence of HCl gas. Table 3 summarizes the values obtained for ΣN_{fs} and $\bar{N}_{fs}$ (here, the average midgap fast-state density for n- and p-type Si of a given orientation). The value of $\bar{N}_{fs}$ is seen to depend on orientation, whereas ΣN_{fs} is independent of orientation. The presence of HCl gas during the deposition reduces ΣN_{fs} but increases $\bar{N}_{fs}$ slightly.

In general, N_{fs} for CVD SiO_2 is as low as that for thermal SiO_2 on (100) Si, and about an order of magnitude lower than that for thermal oxide on (111) Si. This latter fact could prove to be highly useful for three-dimensional IGFETs, such as VMOS (vertical MOS) [11] devices.

Summary and conclusions

The CVD SiO_2 deposition system and the physical properties of the resulting oxides have been described. Unannealed CVD SiO_2 has been shown to be as good as unannealed thermal SiO_2 on (100) Si and better than unannealed or annealed thermal SiO_2 on (111) Si. Specifically,

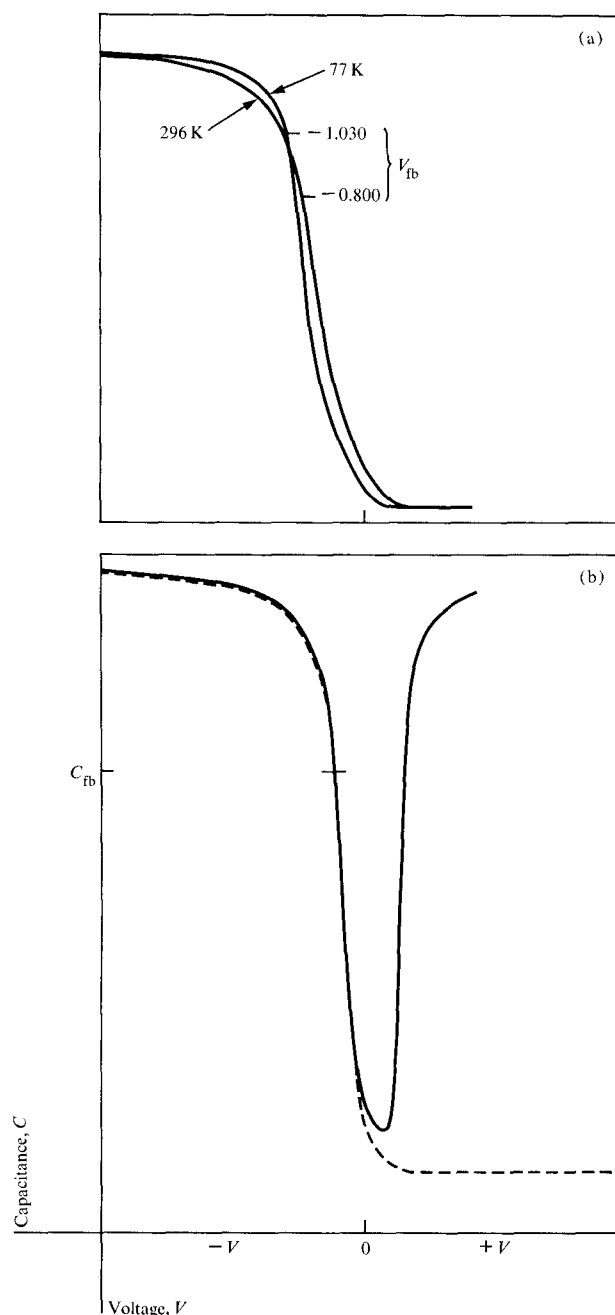


Figure 3 (a) Typical 1-MHz (high-frequency) capacitance-voltage (C - V) curves at 296 and 77 K for MOS structures with CVD SiO_2 on p-type Si, showing the temperature dependence of V_{fb} . (b) Typical room-temperature low-frequency (—) and high-frequency (---) C - V curves for MOS structures with CVD SiO_2 used to determine N'_{fs} ; 48.6-nm oxide film on (100) p-type Si, $N'_a = 8 \times 10^{15}/\text{cm}^3$.

excellent control of the fixed-charge and fast-surface-state densities has been demonstrated, with considerable latitude achievable in these two properties. We have been able to eliminate distributed bulk charge on (100) Si and eliminate or reduce the value of Q_{ic} to $<6 \times 10^{10} \text{ cm}^{-2}$ on

Table 3 Total fast-state density $\Sigma N'_{fs}$ and average midgap fast-state density $\bar{N}'_{fs}$ for CVD SiO_2 on (100) and (111) Si.

Orientation	$\Sigma N'_{fs} (10^{10} \text{ cm}^{-2})$		$\bar{N}'_{fs} (10^{10} \text{ cm}^{-2} \cdot \text{eV}^{-1})$	
	No HCl	HCl	No HCl	HCl
(100)	3.3	1.7	1.1	1.8
(111)	3.25	1.8	1.5	2.65

(111) Si. In addition, N'_{fs} has been reduced to $2 \times 10^{10} \text{ cm}^{-2} \cdot \text{eV}^{-1}$ for (100) Si and $3 \times 10^{10} \text{ cm}^{-2} \cdot \text{eV}^{-1}$ for (111) Si. We conclude that near-ideal SiO_2 and Si- SiO_2 interfaces have been fabricated using the CVD SiO_2 -HCl system.

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